REMARKS

Claims 59-61 are added. As a result, claims 11-21 and 59-61 are now pending in this application.

Applicant respectfully requests reconsideration of the above-identified patent application as amended and in view of the following remarks.

§102 Rejection of the Claims

Claims 11-21 were rejected under 35 USC § 102(b) as being anticipated by Manning (U.S. Patent No. 5,652,724). Applicant traverses the rejection, and respectfully submits that Manning does not teach each and every element of the claims, and as such cannot support the rejections.

The Office Action fails to show the elements of the claims. Column 3, lines 27-28 and column 7, lines 61-64 make no mention whatsoever of patternless and patterned addressing schemes. The text of lines 27-28 reads as follows: "The load on each /CAS is typically less than the load on the other control signals ..." Applicant can find no teaching of patternless and patterned addressing schemes in the discussion of the load on a /CAS signal. Lines 61-64 read exactly as follows: "A preferred embodiment of a sixteen bit wide burst EDO MODE dram designed in accordance with the teachings of this invention has two column address strobe input pins /CASH and /CASL." This does not disclose the elements of the claims.

Further, the assertion in the Office Action of the patterned addressing scheme for sequenced CAS being shown in Figure 1, numbers 26 and 30 and the patternless addressing scheme for random CAS at column 3, lines 28-30 is not understood, as numbers 26 and 30 are the column address counter and a column address decoder. Column 3, lines 27-30 state in full: "The load on each /CAS is typically less than the load on the other control signals (/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus." There is no teaching in these passages of Manning of any patternless or patterned addressing scheme.

New claims 59-61 are also believed to define over Manning. Manning does briefly discuss switching between burst EDO and standard EDO modes of operation. However, only a general discussion is present. In Manning, at col. 6, lines 16-22, an initial choice of whether the mode of operation of Manning will be burst EDO or standard EDO is made. The only

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substantive discussion of any switching occurs at col. 6, lines 30-34: "[I]n a device designed with an alternate method of switching between burst and non-burst access cycles, the state of /WE when /RAS falls may be used to switch between other possible modes of operation such as interleaved versus linear addressing modes."

No mention is made in Manning of any control logic or switching circuitry for switching between burst and pipeline data paths as is required by the new claims. The only support for a pipeline mode in Manning is not for a pipeline mode, but instead for a pipeline architecture. This mention of a pipeline architecture does not teach operation of the Manning memory device in either a pipeline or burst mode, and certainly does not teach switching between a burst mode and a pipeline mode of operation.

CONCLUSION

Applicant believes the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims. The Examiner is invited to telephone the below-signed attorney at (612) 373-6904 to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **December 15, 1999**.

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Signature

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